TITLE

SYSTEM FOR INTEGRATING A CIRCUIT ON AN ISOLATION LAYER AND METHOD THEREOF

BACKGROUND OF THE INVENTION

The present invention relates in general to a system for integrating a circuit on an isolation layer and method thereof. In particular, the present invention relates to a method for integrating circuits on different isolation layers and combining the circuits and the isolation layers.

Description of the Related Art

System on glass (SOG) is a low-temperature poly-silicon (LTPS) technology of interest. SOG technology is related to form peripheral circuits on a glass substrate to reduce cost and product size. In general, the cost of a drive IC is 6% of that of a 12-inch SVGA liquid crystal display (LCD). Thus, the low cost of a drive IC manufactured by LTPS technology is a vantage on marketing.

SONY corporation recently disclosed a video system on glass at Europe Display conference (EDC) in 2002. The video system forms the driving circuit of the LCD panel on glass by LTPS technology. FIG. 1 is a circuit diagram showing the driving circuit of a LCD panel, comprising gate driver 10, interface circuit 12, timing generator 14, reference driver 16, DC-to-DC converter 18 and source driver 19. Power consumption of the driving circuit is reduced because additional ICs are omitted. Additionally, Sharp and Philips have disclosed similar panel technology. Moreover, Sharp has disclosed the ability to form

a CPU on glass. Fujitsu and Seiko corporations have also recently disclosed similar technologies respectively at Society for Information Display (SID) and International Display Works (IDW) conference in 2002. Thus, the combination of CPU and memory on glass by LTPS technology is anticipated.

However, reliability is a serious concern when mass producing SOG products. Since circuits with different process parameters are combined and manufactured together in a single system, problems occurring in any individual circuit affect the entire system. Thus, the reliability of the products manufactured by SOG technology is seriously diminished.

U.S. application 20020126108A1 provides a method for forming the CPU, the memory, the control circuit and the display device on at least two substrates, and mounting the substrates on one of the substrate. Thus, the product reliability is increased, but the size, especially the thickness, of the product is also increased.

SUMMARY OF THE INVENTION

The object of the present invention is thus to provide a method for integrating a system on an isolation layer by individually forming different kinds of circuits, including display circuits, control circuits, CPUs and memory circuits, on different isolation layers, after cutting the isolation layers and leaving an individual circuit on the cut isolation layer, the cut isolation layer and the individual circuit are combined with others isolation layers and circuits thereon. In addition, the manufacturing processes, design rules, package methods and

radiator methods of the circuits are selected according to their characteristics.

To achieve the above-mentioned object, the present invention provides a method for integrating a system on an isolation layer. A first isolation substrate including a first circuit deposition region and a first substrate-combining region, and a second isolation substrate including a second circuit deposition region and a second substrate-combining region are provided. Next, a first circuit and a second circuit are respectively formed on the first circuit deposition region and the second circuit deposition region. Next, substrate-connecting elements are formed to connect the first substrate-combining region to the second substrate-combining region. Finally, electrical connecting elements are formed to electrically connect the first circuit and the second circuit.

In addition, the present invention provides a system for integrating circuitry on an isolation layer. A plurality of isolation substrates, including a circuit deposition region and a substrate-combining region are provided. A plurality of circuits is formed on the circuit deposition regions. A plurality of substrate-connecting elements is formed to connect the substrate-combining regions. A plurality of electrical connecting elements is formed to electrically connect the circuits formed on the different circuit deposition regions.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

FIG. 1 is a circuit diagram showing the driving circuit of a LCD panel.

FIG. 2 is a flowchart illustrative of integrating a system on an isolation layer according to the embodiment of the present invention.

FIG. 3 shows the outer views of the isolation substrates 20A and 20B.

FIG. 4 shows the outer views of the cut isolation substrate and the circuit block thereof.

FIGs. 5A and 5B show the circuit blocks are connected by the electrical connecting elements.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 is a flowchart illustrative of integrating a system on an isolation layer according to the embodiment of the present invention. First, a plurality of isolation substrates is provided (S1). The material of the isolation substrates can be plastic or glass. Here, the material of the isolation substrate is determined according to the following manufacturing process. FIG. 3 shows the outer views of the isolation substrates 20A and 20B. As shown in FIG. 3, the arrow indicates the circuit deposition region. Next, a plurality of circuits is formed on the circuit deposition regions 21 of the isolation substrates 20A and 20B, respectively (S2). The circuits can be power converting

circuits, memory circuits, logic control circuits, CPUs, display panels, and driving circuits for driving the panel. For example, the power converting circuit POWER is formed on the isolation substrate 20A and the CPU is formed on the isolation substrate 20B. In the present invention, the circuits on the single isolation substrate can be formed by the same manufacturing process. For example, if the circuits are all formed by a CMOS process, the circuits can be formed together on a single isolation substrate. In addition, the electrical elements having different process parameters are formed on different isolation substrates, for example, the thickness of gate oxide layers of memory devices and periphery circuits are different. In addition, circuits formed by the processes requiring different numbers of masks, circuits with different design rules, package methods and radiator methods are formed on different isolation substrates to simplify the manufacturing process. In the present invention, a plurality of circuits is formed on a single isolation substrate. As shown in FIG. 3, there are a plurality of power converting circuits POWER formed on isolation substrate 22A and the CPU blocks formed on isolation substrate 22B. Next, the isolation substrates 20A and 20B are cut along cutting lines 24A and 24B (S3). As shown in FIG. 4, only the single CPU block is left on the cut isolation substrate 20B. The top surface of the cut isolation substrate 20B is a circuit deposition region 21, which is deposited on the CPU block, and the side surfaces 26 of the cut isolation substrate 20B contiguous to the circuit deposition region 21 are substrate-combining regions. Next, a plurality of substrate-connecting elements is formed to connect the cut isolation substrates (S4), wherein the substrate-combining regions contact of the cut isolation substrates. Here, the

substrate-connecting elements can be viscose, or formed by laser or heat fusion. Finally, a plurality of electrical connecting elements is formed to electrically connect the circuits on different isolation substrates (S5). FIGs. 5A and 5B show the circuit blocks connected by the electrical connecting elements, wherein the isolation substrates are in contact. In the embodiment of the present invention, the electrical connecting elements are flex print cables (shown in FIG. 5A), gold lines (shown in FIG. 5B), or formed by laser fusion.

According to the system for integrating a circuit on an isolation layer and the method thereof disclosed by the embodiment of the present invention, the thickness of the system is reduced because the isolation substrates are joined by the side surfaces thereof. Thus, the disadvantage of the method disclosed by U.S. application 20020126108A1 is avoided. In addition, the method disclosed by the present invention forms the electrical elements with different process parameters on the different isolation layers. The isolation layer and the electrical elements are then respectively combined with other isolation layers and the electrical elements thereon. Thus, the reliability of the products and the design elasticity of the SOG technology are improved.

The foregoing description of the preferred embodiments of this invention has been presented for purposes of illustration and description. Obvious modifications or variations are possible in light of the above teaching. The embodiments were chosen and described to provide the best illustration of the principles of this invention and its practical application to thereby enable those skilled in the art to utilize the invention

in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the present invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.